REMARKS/ARGUMENTS

Prior to this amendment claims 3-6, 9-11, 13-17, 19, and 21-33 were pending. By this amendment, claims 5, 6, 14, and 15 are amended, leaving claims 3-6, 9-11, 13-17, 19, 21-33 pending consideration. Claims 3, 4, 9-11, 13, 17, 19, and 21-33 are allowed. Claims 5 and 14 stand rejected under 35 USC §103(a) over U.S. Patent No. 6,529,041 issued to Ng et al. (hereinafter "Ng") in view of U.S. Patent No. 6,710,621 issued to Devlin et al. (hereinafter "Devlin"). Claims 6 and 15 stand rejected under 35 USC §103(a) over Ng in view of U.S. Patent No. 6,232,893 issued to Cliff et al. (hereinafter "Cliff"). Applicants aver that no new matter is added in this response.

§103 Rejections

In the Office Action, the Examiner rejected claims 5, 6, 14, and 15 under 35 USC § 103(a), stating claims 5 and 14 are anticipated by Ng in view of Devlin, and claims 6 and 15 are anticipated by Ng in view of Cliff. For at least the reasons stated below, the Applicants respectfully request reconsideration and withdrawal of the rejections, as each of the claims as amended are patentable over Ng alone or in combination with Devlin, or Ng alone or in combination with Cliff.

Claims 5 and 14

With regard to claims 5 and 14, in the Office Action the Examiner stated that Ng discloses a programmable logic device having an active logic section, a configuration memory having separate power supply connections and points to figures 1-4 of Ng, but also states that Ng does not disclose a programmable input/output section. In the Office Action, the Examiner states that Devlin discloses a separate power supply connection. The Applicants respectfully submit that this assertion does not adequately show that all of claim limitations are taught or suggested in Ng alone or in combination with Devlin.

The Applicants submit that Ng alone or in combination with Devlin fails to disclose all the elements of claims 5 and 14. For example, amended claim 5 recites in part "each

of the separate power supply connections for the active logic section, the configuration memory, and the programmable input/output section are selectable between at least two different voltage levels", and claim 14 recites in part , "the power supplied to the configuration memory or to the programmable input/output section comprises at least two selectable voltage levels."

Ng discloses a power control device (PCD) to supply a voltage VCC to a memory (SRAM), a PLD, and a CPU. Ng discloses input/output blocks (IOB) designed to eliminate the need for the PCD. The I/O blocks as described in Ng use data output signals to provide two functions, one function of the IOB provides a low current state for normal input/output data communication, a second function of the IOB provides a high current state for driving an IC device (Ng, Figs 1-9, col. 4, line 64 to col. 5, line 12).

Devlin discloses a voltage supply system designed to supply different power supply voltages thereby allowing FPGAs having different power supply voltage requirements to be mounted to a configurable daughterboard that connects to a common motherboard. The voltages are derived from a programmable power supply external to the daughterboards and the FPGA. It is apparent from the teaching of Devlin that Devlin's power supply system is intended to provide programmable voltages to allow the forward and backward compatibility of different FPGAs and daughterboard combinations (Devlin, Figs. 2-6, abstract, col. 3 lines 5-40).

As Ng teaches away from using a power control device, and Devlin teaches a separate power control device (i.e., a separate programmable power supply), Ng and Devlin cannot be properly combined as there is no motivation to do so. However, even if Ng and Devlin could be combined, there is nothing in Ng alone or in combination with Devlin that discloses or suggests separate power supply connections for the active logic section, the configuration memory, and the programmable input/output section that are selectable between at least two different voltage levels, as recited in amended claim 5, nor power supplied to the configuration memory or to the programmable input/output section comprises at least two selectable voltage levels as recited in amended claim 14. Claims 5 and 14 are thus patentably distinguished over Ng alone or in combination with Devlin for at least the above reasons.

Claims 6 and 15

With regard to claims 6 and 15, in the Office Action the Examiner stated that Ng discloses a programmable logic device having an active logic section, a configuration memory having separate power supply connections and points to figures 1-4 of Ng, and also states that Ng does not disclose the configuration memory has power supply connections at two different voltages. In the Office Action, the Examiner states that Cliff discloses configuration memory that has power supply connections to power supplies at two or more different voltages. The Applicants respectfully submit that this assertion does not adequately show that all of claim limitations are taught or suggested in Ng alone or in combination with Cliff.

The Applicants submit that Ng alone or in combination with Cliff fails to disclose all the elements of claims 6 and 15. For example, claim 6 recites in part the "active logic section and the configuration memory have separate power supply connections", and "the separate power supply connections are selectable between a first voltage level and a second voltage level lower in value than the first voltage level", and claim 15 recites in part "the power supplied to the active logic section or to the programmable input/output section comprises at least two selectable voltage levels."

As described above, Ng discloses input/output blocks (IOB) designed to eliminate the need for a separate power control device. Cliff discloses a separate programmable voltage regulator used to convert an input voltage to a desired operating voltage for individual PLDs (Cliff, Fig. 3, col. 3 lines 9-43, col. 6, lines 11-30).

As Ng teaches away from using a power control device, and Cliff teaches a separate power control device (i.e., a programmable voltage regulator), Ng and Cliff cannot be properly combined as there is no motivation to do so. However, even if Ng and Cliff could be combined, there is nothing in Ng alone or in combination with Cliff that discloses or suggests an active logic section and a configuration memory having separate power supply connections that are selectable between a first voltage level and a second voltage level lower in value than the first voltage level as recited in amended claim 6, nor power supplied to the active logic section or to the programmable input/output section comprises at least two selectable voltage levels as

recited in amended claim 15. Claims 6 and 15 are thus patentably distinguished over Ng alone or in combination with Cliff for at least the above reasons.

Dependent Claim 16

Claim 16 depends from amended claim 15 and is therefore patentable for at least the above reasons. Claim 16 however recites additional elements that further distinguish over the cited art. For example, claim 16 recites supplying a first voltage to the configuration memory in said normal mode of operation and supplying a second voltage, lower than said first voltage, to the configuration memory in said first mode of operation. Claim 16 is thus patentably distinguished over Ng alone or in combination with Cliff for at least the above reasons.

Allowable Subject Matter

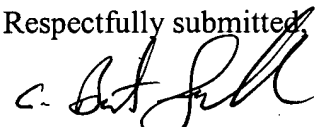
Applicants note with appreciation allowance of claims 3, 4, 9-11, 13, 17, 19, and 21-33.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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